Focus Group on Quantum Technologies

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TITLE	**Cleaning-up annex E on Cryogenic Solid State QC**
PROJECT	FGQT Roadmap
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ABSTRACT

The content of chapter 8 (quantum computing and simulation) has organically grown during time, while we where developing relevant content. Annex E is dedicated to identify further details on a particular architecture: *cryogenic solid state quantum computing*. Its purpose is to collect good ideas for future standards

Now consensus has been achieved on the content of chapter 8, the content of Annex E should follow accordingly.

This contribution proposes a significant clean-up of the introductory parts of Annex E, particularly with future standardisation in mind. Its structure and introduction may serve as a starting point for a first standard on cryogenic solid state quantum computing, to be elaborated within CEN/CENELEC by the recently established JTC (Joint Technical Comity)

Literal text proposal for annex „E“

Annex E: Cryogenic Solid-state Quantum Computing

E.1 Scope and objectives

The scope of this annex are the hardware layers and control software dedicated to cryogenic solid state quantum computing. This is an architecture family of which all members make use of a cryogenic fridge, and where the quantum device(s) are controlled from outside the fridge by room-temperature control electronics. Consequently, a huge number of I/O channels is required to interconnect the qubits within these quantum devices with room temperature electronics.
So far, the following members have been identified within this architecture family: superconducting transmons, superconducting flux qubits, semiconductor spin qubits, topological qubits and artificial atoms in solids.

The objective is to create a first document, out of a series of documents, that is restricted to provide functional descriptions of the involved layers and to identify associated functional requirements. The specification of limiting requirements and associated values is explicitly out-of-scope of this first document. On the other hand, descriptions of multiple best-practices on implementations are within scope as long as their description does not exclude similar other solutions.
As such, this annex may serve as a good starting point for collecting ideas to feed initial standards on cryogenic quantum computers.

E.2 References

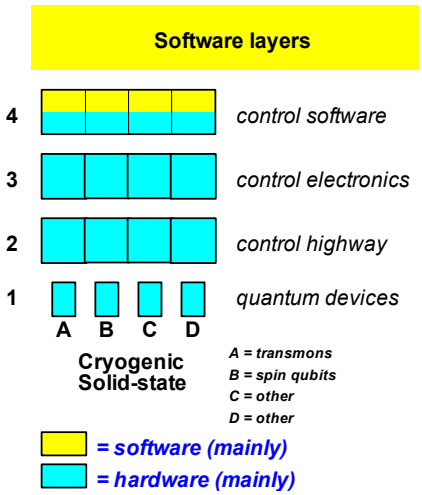
[1] FGQT Standardization Roadmap, CEN-CENELEC nr xxxx, 2023
[2] …

E.3 Terminology and abbreviations

E.3.1 Terminology

For the purposes of the present document, the following terminology and definitions apply:

Hardware stack – A layered description of functionality covering a specific quantum computing architecture family accounting for different members. Cryogenic solid-state quantum computers is an example of such an architecture family, and implementations based on transmons and spin-qubits are examples of its members. Where needed, a layer may distinguish between different solutions for different members, and may consist of hardware and/or (low level) software.



Quantum devices – The modules in hardware layer 1 that are typically operating at cryogenic temperatures and may be implemented as chip and/or on PCB.

Control highway – The modules in hardware layer 2 that cover all infrastructure needed for transporting microwave, lightwave, RF and DC signals (via electrical and/or optical means) between the control electronics at room temperature and the quantum devices at cryogenic temperatures. It is a mix transmission lines, filtering, attenuation, amplification, (de)multiplexing, etc. A huge number of control channels are required to control many qubits in a single fridge (which clarifies the name) and this can easily become very bulky.

Control electronics – The modules in hardware layer 3 that covers all room-temperature electronics for generating, receiving, and processing microwave, lightwave, RF and DC signals. Some implementations make use of routing/switching and/or multiplexing of control signals at room temperatures. It may have some firmware on board to guide the signal generation and signal processing.

Control software – The modules in layer 4, which can be a mix of hardware and low-level driver software, for instructing the control electronics. It may also have means to enable calibrating and bench marking purposes. It has a software interface to higher layers for receiving sequences of instructions about when, where and what pulses are to be generated.

E.3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

FGQT – CEN/CENELEC Focus Group on Quantum Technology
PCB – Printed Circuit Board
DC - Direct Current
RF – Radio Frequent

E.4 Overview of concepts

[use the existing content of the present section E.5 “Overview of concepts”]

E.5 Layer 1 - Quantum Devices

Quantum devices of cryogenic solid state quantum computers are typically operating at cryogenic temperatures. They may be implemented stand-alone, as chip and/or on PCB. This section is currently a place holder for functional descriptions and associated functional requirements, to be elaborated in further detail during a follow-up activity.

The functional requirements may identify topics such as materials compatibility, shielding, operating temperature, electrical and magnetic aspects, vacuum properties, etc.

E.6 Layer 2 - Control Highway

[use the existing content of the present section E.6 “Control Highway”]

E.7 Layer 3 - Control Electronics

The control electronics is primarily intended for generating the desired pulses to control the quantum devices in layer 1, and to read-out their response. It covers all room-temperature electronics for generating, receiving, and processing microwave, lightwave, RF and DC signals. Some implementations make use of routing/switching and/or multiplexing of control signals at room temperatures. It may have some firmware on board to guide the signal generation and signal processing.

This section is currently a place holder for functional descriptions and associated functional requirements, to be elaborated in further detail during a follow-up activity.

The functional description may include the blocks for generating and detecting pulses, as well as for multiplexing and/or routing/switching functionality (when appropriated). It may also describe various best-practices on interfacing with the Control Software in layer 4.

The functional requirements may identify topics such as signal levels, pulse shapes, noise, sensitivity, dynamic range, etc.

E.8 Layer 4 - Control Software

This layer covers hardware-specific software to control what pulses are to be generated by the control electronics in layer 3, and also covers all kinds of means for calibration and bench marking the system as a whole and how to interface with higher software layers.

This section is currently a place holder for functional descriptions and associated functional requirements, to be elaborated in further detail.

The functional description may include the needs for enabling calibration and bench marking

End of literal text proposal for annex „E“